Reg. No. :

Question Paper Code : 51207

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2013.

Third Semester

Electronics and Communication Engineering EC 1201 — DIGITAL ELECTRONICS

(Regulation 2008)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — $(10 \times 2 = 20 \text{ marks})$

- 1. Define bit, byte and nibble.
- 2. Find the complement of $A\overline{B} + \overline{B}C + C\overline{D}$.
- 3. What do you mean by weighted code? Give example.
- 4. Draw the symbol and Truth Table for J-K filp-flop.
- 5. Draw the logic circuit for the expression $F = \overline{x} \overline{y} z + \overline{x} y z + x \overline{y}$.
- 6. Define modulus of a counter.
- 7. Give significance of priority encoder.
- 8. Distinguish between EPROM and EEPROM.
- 9. What is universal shift register?
- 10. What is the difference between static and dynamic RAM?

PART B — $(5 \times 16 = 80 \text{ marks})$

- 11. (a) (i) Design the circuit for one bit comparator. (8)
 - (ii) Design a full adder circuitusing NAND gates only.

(8)

Or

- (b) (i) Write a detailed technical note on the Hardware Description Language. (8)
 - (ii) What is Karnaugh Map? A truth table has output 0 for input ABCD = 0000, 0010, 1100, 1101, 1110, 1111, 0101, 0111. Simplify using karnaugh Map & draw the simplified circuit.

12. (a) Draw the circuit of TTL NAND gate and explain its operation. Compare the TTL and ECL logic families. (16)

Or

- (b) (i) Write a detailed technical note on the interfacing of CMOS and TTL families. (8)
 - (ii) Explain the switching operation and characteristics of PN junction diode.
 (8)
- 13. (a) (i) Implement the following function using 3 to 8 decoder. (8)

$$f(A, B, C) = \sum m (O, 1, 4, 5, 7)$$

14.

(ii) Discuss in detail, about the multiplexer and demultiplexer as logic elements with examples.
 (8)

Or

(b)	(i)	Explain the combinational logic design using MSI devices.	(6)
	(ii)	What is the importance and applications of Gray code? Convert binary number 10100111 to Gray code.	the (6)
	(iii)	Explain 1-bit magnitude comparator.	(4)
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(a)	(i)	Design a synchronous decade counter to count in the follow sequence. 1, 0, 2, 3, 4, 8, 7,6, 5.	ing (8)
	(ii)	What is sequential circuit? Explain S-R and J K flip flop.	(8)
		Or	
(b)	(i)	Draw and explain 4-bit synchronous Up / Down counter.	(8)
	(ii)	Design a serial 2's complementer with a shaft register and fin flop. The binary number is shifter out from one side and its	l a

- (ii) Design a serial 2's complementer with a shart register and a flip-flop. The binary number is shifter out from one side and its 2's complement shifted into the other side of the shift register. (8)
- 15. (a) (i) Draw the circuit of a BJT RAM cell and explain its operation. (8)
 - (ii) Give the classification of memory and explain the block diagram of ROM. (8)
 - Or

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(b)	Alon	g with neat diagrams write a detailed technical note on the follow	ving
	(i)	MOSFET RAM cell.	(8)
1	(ii)	FPGA,	(8)